A Comparative Analysis of Nonlinear Current Control Schemes Applied to a SEPIC Power Factor Corrector

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Abstract – In this paper, a comparative analysis of two nonlinear control schemes proposed for a Single Ended Primary Inductance Converter (SEPIC) Power Factor Corrector (PFC) is presented. The SEPIC converter, compared to conventional buck or boost ones, allows a low current ripple at the input for a relatively low level of the DC-bus voltage. Consequently, the high frequency filter needed at the AC-side of a buck converter is avoided, and the high voltage stresses applied on the switches are significantly reduced with respect to the boost converter. The converter is integrated at the DC-end of a single-phase diode bridge. In order to ensure a unity power factor at the AC-source side and a regulated voltage at the DC-load side, a multiple-loops feedback control scheme has to be developed. Two control strategies are considered in this paper. The first one uses a robust hysteresis current controller, whereas the other method is based on the application of the input/output feedback linearization technique on a state-space averaged model of the converter. In order to verify and compare the performance of both control schemes, numerical simulations are carried out on a switching-functions-based model of the converter, which is implemented using Matlab/Simulink. The proposed model of the converter is valid in the Continuous Current Mode (CCM) and the Discontinuous Current Mode (DCM). The control systems are tested under both rated and disturbed operating conditions. The systems performance is evaluated in terms of source current Total Harmonic Distortion (THD), input power factor, DC voltage regulation and robustness toward a load disturbance.

I. INTRODUCTION

High power quality is increasingly required for the power supply systems in order to comply with the international standards [1]. For this purpose, and especially for single-phase low power applications, switch-mode DC-DC converters, commonly known as Power Factor Correction (PFC) circuits, are designed in order to ensure a high power factor at the mains side, and to emulate a purely resistive operation of the diode-bridge-based front-end rectifier [2].

Three families of PFC exist in the literature: the Buck [3], the Boost [4] and the Buck-Boost [5] topologies. The Buck topology is characterized by a low DC voltage at the output, but a high frequency commutated current at the input. Due to the discontinuous nature of the input current, the Buck converter has to be connected to an ultra-fast-recovery diode bridge when it is used as a PFC circuit. Although the low voltage stresses it may exhibit, a Buck PFC has a major drawback that is the necessity of a high frequency shunt filter to be inserted between the source and the diode bridge.

On the other hand, the Boost-type topology presents a smoothly varying input current (due to the presence of a filtering inductor), but a relatively high DC-bus voltage (at least the peak value of the source voltage) that may cause over-voltage stresses on the switches. In addition, and contrarily to the Buck PFC, the front-end diode bridge operates in continuous current mode at the mains frequency (60Hz) and, therefore, the presence of a high-frequency filter at the AC-side is no more necessary.

The third family of PFC concerns Buck-Boost combinations, in which the most suitable topologies for power factor correction are the Cuk converter [6] (Fig. 3.c) and the Single Ended Primary Inductance Converter (SEPIC) [7] (Fig. 3.d). These two converters differ from each other at the output stage, where the free-wheel diode and the output inductor are permutated, and the polarity of the output voltage is inverted. In both cases, the DC voltage delivered at the output can vary theoretically between zero and an infinite value.

In this paper, a SEPIC-type PFC circuit is adopted for improving the power factor at the input side of a single-phase diode rectifier, as described in Fig. 1. The main switch is controlled by a multiple-loops control scheme in order to ensure a line current wave-shaping and a DC load voltage regulation.

![Fig. 1. Buck-Boost SEPIC power factor correction circuit.](image)

Two methods are considered for the design of the control scheme. The first uses a robust hysteresis current controller [9], whereas the second is based mainly on the input/output feedback linearization technique [8]. The performance of
both control schemes is then analysed through numerical simulations by using the Matlab/Simulink tool. For this purpose, a general-case switching-function-based mathematical model of the converter is implemented, and the control process is launched under different operating conditions in order to test successively the dynamics, the robustness and the tracking abilities of the controllers.

II. OPERATION SEQUENCES AND SWITCHING-FUNCTION-BASED MODEL

The operating sequences of the SEPIC converter in the most general case of a Discontinuous Current Mode (DCM) are summarized in Fig. 2. The circuit has three possible configurations, depending on the state of the main switch \( Q \) and diode \( D \). The third configuration, where both \( Q \) and \( D \) are at their off-state, appears only when the current \((i_{L1} + i_{L2})\) crosses zero. Otherwise, i.e. if the condition \((i_{L1} + i_{L2}) > 0\) always stands, only the first two configurations exit in a switching period. In that case, the converter is said to operate in a Continuous Current Mode (CCM), and the diode \( D \) will always conducts whenever the switch \( Q \) is turned-off. Following these considerations, we may describe analytically the operation of the converter in the more general case by writing the equations (1) given at the bottom of this page, where \( s_Q \) denotes the switching function of switch \( Q \), defined as:

\[
s_Q = \begin{cases} 
0 & \text{if } Q \text{ is turned-off} \\
1 & \text{if } Q \text{ is turned-on} 
\end{cases}
\]  

\( \theta \) is the threshold function defined as:

\[
\theta(z) = \begin{cases} 
0 & \text{if } z \leq 0 \\
1 & \text{if } z > 0 
\end{cases}
\]

\( s_Q \) and \( \bar{s}_Q \) their respective complements.

Note that in CCM the \( \theta(i_{L1} + i_{L2}) \) term is always equal to unity, and the model (1) becomes simpler. Moreover, the switching frequency of switch \( Q \) is either time-varying (if a hysteresis flip-flop controller is used for the line current shaping) or fixed (if a saw-tooth-carrier-based pulse-width modulator is used along with a continuous current controller). However, it will be assumed in both cases, especially as far as the calculation of the reactive components \( L_1, L_2, C \) and \( C_0 \) (detailed in [9] and [10]) is concerned, that the lowest switching frequency is far beyond the bandwidth of the current and voltage loops. Consequently, a simplified averaged model of the converter may be adopted in order to analyse the low-frequency operation of the converter in the steady-state regime and to choose, thus, the required reactive components.

III. CONTROL SYSTEM DESIGN

The control circuit is depicted in Fig. 3. It consists of two successive loops: the inner or current one is designed to ensure the wave-shaping of the DC input current \( i_{L1} \) and, consequently, the improvement of the input power factor, while the outer or voltage loop is aimed to regulate the DC load voltage and to stabilize it around a desired set-point. The inner current controller is designed by two different methods. In the first approach, a simple hysteresis controller is used for the current shaping, whereas in the second approach, it is based on the Single-Input-Single-Output (SISO) input/output feedback linearization principles in order to achieve nonlinearity compensation of the inner subsystem. The outer voltage regulator is chosen to be a linear Proportional-Integral (PI) one for both control schemes. \( K_i \) and \( K_v \) are scaling gains. To ensure high stability of the control system, the outer loop is designed to be enough slower than the inner one. In addition, in order to emulate a pure resistor behavior, the current reference must have the same shape as the rectified source voltage \( v_{in} \), with an adjustable magnitude. An analog multiplier is used for this purpose. Furthermore, in order to avoid the distortion of the current reference, the voltage control signal \( u_c \) should be harmonic-free. This can be satisfied by inserting a suitable second-order low-pass filter, represented by the transfer function \( F_c(s) \), in the voltage feedback path.

A. Hysteresis-Based Inner Controller

This first design approach uses a hysteresis flip-flop controller for the input current shaping, as illustrated in Fig. 4.a [9]. The switching frequency is time-varying, and the high-frequency current ripple is fixed by the hysteresis width \( h \). The value of \( h \) will be chosen in order to have a maximum value of the switching frequency equal to 40kHz. It yields: \( h = 0.6 \).

\[
\begin{align*}
L_1 \frac{di_{L1}}{dt} &= s_Q \cdot v_{in} + s_Q \cdot \theta(i_{L1} + i_{L2}) \cdot (v_m - v_c) + s_Q \cdot \theta(i_{L1} + i_{L2}) \cdot \frac{L_1}{L_1 + L_2} \cdot (v_m - v_c) \\
L_2 \frac{di_{L2}}{dt} &= s_Q \cdot v_c - s_Q \cdot \theta(i_{L1} + i_{L2}) \cdot v_0 - s_Q \cdot \theta(i_{L1} + i_{L2}) \cdot \frac{L_2}{L_1 + L_2} \cdot (v_m - v_c) \\
C \frac{dv_c}{dt} &= -s_Q \cdot i_{L1} - s_Q \cdot i_{L2} \\
C_0 \frac{dv_0}{dt} &= s_Q \cdot \theta(i_{L1} + i_{L2}) \cdot (i_{L1} + i_{L2}) - i_0
\end{align*}
\]  

(1)
B. Averaged-Model-Based Feedback Linearizing Controller

Here, the SISO input/output feedback linearization technique is applied for the design of the inner control law [8]. The inner control scheme is depicted in Fig. 4.b. A carrier-based modulator is employed, which implies a fixed-switching-frequency operation mode. \( T \) denotes the nonlinear input transformation inherent to the applied feedback linearization scheme.

The design of the feedback linearizing control law is based on the knowledge of an averaged model of the converter [10]. Applying the state-space averaging modelling technique to system (1) in CCM mode (it is assumed here that the condition \((i_{L1}^* + i_{L2}^*) > 0\) always stands; this assumption is justified by a suitable choice of inductor \(L_2\) [9-10]) yields the following required model of the converter, where \(d(t)\) denotes the duty cycle of the switch \(Q\):

\[
\begin{align*}
L_1 \frac{di_{L1}}{dt} &= v_{in} - (1-d) \cdot (v_C + v_0) \\
L_2 \frac{di_{L2}}{dt} &= d \cdot v_C - (1-d) \cdot v_0 \\
C \frac{dv_C}{dt} &= (1-d) \cdot i_{L1} - d \cdot i_{L2} \\
C_0 \frac{dv_0}{dt} &= (1-d) \cdot (i_{L1} + i_{L2}) - i_0
\end{align*}
\]

(4)

The relative degree of system (4) is 1. Thus, the derivation of the inner control law is based on the first equation in (4). It yields:

\[
d = \frac{1}{2} \left( \frac{u_i}{v_{PWM}} \right) = \frac{L_1 v_i - v_{in} + v_C + v_0}{v_C + v_0}
\]

(5)

or:

\[
u_i = T(v_i) = \frac{2L_1 v_i - 2v_{in} + v_C + v_0}{v_C + v_0} \cdot v_{PWM}
\]

(6)

where \(u_i\) denotes the output of the inner controller, \(v_i\) the new control input of the linearized inner subsystem, and \(v_{PWM}\) the peak value of the saw-tooth modulation signal. Replacing equation (5) into model (4) gives the following canonical form of the inner subsystem:

\[
\frac{di_{L1}}{dt} = v_i
\]

(7)

For the tracking problem at hand, we may choose the following control law:

\[
v_i = \frac{di_{L1}^*}{dt} - k(i_{L1} - i_{L1}^*) \quad \text{with} \quad k > 0
\]

(8)

The internal dynamics are characterized by a third-order subsystem. By assuming \(i_{L1}\) identically zero, and neglecting the disturbance input \(v_{in}\), it is easily found that all the eigenvalues of this subsystem are in the left-half plane and, thus, the zero-dynamics of system (4) are stable.

IV. NUMERICAL IMPLEMENTATION AND SIMULATION RESULTS

In order to highlight the performance of the SEPIC converter in PFC applications using the proposed control laws, a virtual version of the control system of Fig. 3 has been implemented using the Simulink tool of Matlab. The numerical values of the structural parameters and operating conditions are given in the appendix. The converter is implemented according to the general equations given in (1). This model is valid both in CCM and DCM operations. The simulations are carried out using a fixed-step ode5 (Dormand-Prince) solver. The step size is 1µs.

Fig. 5 illustrates the waveforms of the system variables in the steady-state regime for a 1kW-load when the hysteresis-based current controller is used. The line current THD is 8.64% and the power factor is 0.995. This relatively high level of current distortion is due mainly to the control detuning phenomenon that could appear at the zero crossings of the current (see Fig. 5.a). In fact, at the close neighborhood of the current zero crossings, the line voltage has very small values; consequently, the current reference may become unreachable and the current wave-shaping capability could be lost. Furthermore, the switching frequency is time-varying; it lies between 3.5kHz (at the zero crossings of the line current \(i_0\)) and 36kHz (at the positive and negative peaks of \(i_0\)). The DC output voltage \(v_0\) is stabilized at the reference value of 100V, with a 2.5% ripple at 120Hz (twice the mains frequency). The voltage of the intermediate capacitor \(C\) is also stabilized at 108V, with a 2.2% ripple at 120Hz. Fig. 6 presents the response of the system to a 50% decrease of the load power using the same
controllers as above. The control system still exhibits a low current THD and a high power factor. In addition, the output voltage returns to its desired value in less than 350ms. However, as it is noticed in Figs. 6.b and 6.c, a sub-harmonic at 10Hz exists in the waveforms of $v_0$ and $i_{L2}$ along with the 120Hz-component. This additional distortion is inherent to the dynamics of the outer loop in the control scheme.

Fig. 7 illustrates the waveforms of the system variables in the steady-state regime for a 1kW-load when the averaged-model-based feedback linearizing control is applied. The line current THD is 4.7% and the power factor is 0.999. The switching frequency is fixed at 40kHz; contrarily to the case of a hysteresis inner controller where the switching frequency is time-dependent and varies between 4kHz and 45kHz. In addition, the control detuning problem is inexistent (see Fig. 7.a). The DC output voltage $v_0$ is stabilized at the reference value of 100V, with a 3% ripple at 120Hz. The voltage of the intermediate capacitor $C$ is also stabilized at 108V, with a 2.3% ripple at 120Hz. Fig. 8 presents the response of the system with the same control law to a 50% decrease of the load power. The control system still exhibits a low current THD and a high power factor. In addition, the output voltage returns to its desired value in less than 300ms. We notice again, in Figs. 8.b and 8.c, the presence of the sub-harmonic at 10Hz in the waveforms of $v_0$ and $i_{L2}$ along with the 120Hz-component.

Fig. 9 and Fig. 10 show the spectra of the source current for both control schemes. Note the superiority of the feedback linearizing controller over the hysteresis-based one regarding the harmonic content in both the low-frequency and high-frequency regions.

Fig. 11 and Fig. 12 present respectively the variations of the source current THD and the input power factor with respect to the load power for both control schemes.

V. CONCLUSION

In this paper, a comparative analysis of two multiple-loops control schemes for a SEPIC-type power factor correction circuit, used in single-phase rectifiers, is proposed. The first approach for the control design uses a robust hysteresis current controller, whereas the other approach is based on the application of the input/output feedback linearization technique on a state-space averaged model of the converter. The control systems are both aimed to ensure a low current THD and a high power factor at the AC side, and a regulated load voltage at the DC side. The control schemes were implemented numerically using the Matlab/Simulink tool, and their performance was evaluated both in the steady-state and dynamic regimes.

VI. ACKNOWLEDGMENT

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Fig. 5. Steady-state performance at the rated load using the hysteresis-based inner controller. Waveforms of (a) the voltage and current at the mains, (b) the voltages at the intermediate and load capacitors, (c) the currents in the input and intermediate inductors.

Fig. 6. Regulation performance to a 50% load decrease using the hysteresis-based inner controller. Waveforms of (a) the voltage and current at the mains, (b) the voltages at the intermediate and load capacitors, (c) the currents in the input and intermediate inductors.

Fig. 7. Steady-state performance at the rated load using the averaged-model-based feedback linearizing controller. Waveforms of (a) the voltage and current at the mains, (b) the voltages at the intermediate and load capacitors, (c) the currents in the input and intermediate inductors.

Fig. 8. Regulation performance to a 50% load decrease using the averaged-model-based feedback linearizing controller. Waveforms of (a) the voltage and current at the mains, (b) the voltages at the intermediate and load capacitors, (c) the currents in the input and intermediate inductors.
Fig. 9. Spectrum of the source current in (a) the low-frequency range and (b) the high-frequency range obtained with the hysteresis controller.

Fig. 10. Spectrum of the source current in (a) the low-frequency range and (b) the high-frequency range obtained with the feedback linearizing controller.

VII. APPENDIX: NUMERICAL VALUES OF THE SYSTEM PARAMETERS AND OPERATING SET POINT

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mains voltage RMS-value</td>
<td>$V_S = 120$V</td>
</tr>
<tr>
<td>Rated load power</td>
<td>$P_0 = 1$kW</td>
</tr>
<tr>
<td>Voltage reference</td>
<td>$V_0^* = 100$V</td>
</tr>
<tr>
<td>Mains frequency</td>
<td>$f_0 = 60$Hz</td>
</tr>
<tr>
<td>DC inductors</td>
<td>$L_1 = 1$mH, $L_2 = 10$mH</td>
</tr>
<tr>
<td>Series inductors' resistors</td>
<td>$R_{L1} = 0.1$Ω, $R_{L2} = 0.1$Ω</td>
</tr>
<tr>
<td>DC capacitors</td>
<td>$C = 10$mF, $C_0 = 10$mF</td>
</tr>
<tr>
<td>Scaling gains</td>
<td>$K_i = 1$Ω, $K_v = 1/108$</td>
</tr>
<tr>
<td>Hysteresis controller width</td>
<td>$h = 0.6$</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>$f_s = 40$kHz</td>
</tr>
<tr>
<td>Carrier peak value</td>
<td>$V_{PWM} = 1$V</td>
</tr>
<tr>
<td>Inner current regulator parameter</td>
<td>$k = 30000$</td>
</tr>
<tr>
<td>Outer voltage PI regulator</td>
<td>$H_v(s) = \frac{20}{s} + \frac{15}{s}$</td>
</tr>
<tr>
<td>Voltage filter</td>
<td>$F_v(s) = \frac{0.05}{1 + \sqrt{s}/300 + (s/300)^2}$</td>
</tr>
</tbody>
</table>

VIII. REFERENCES